LP VLSI CASE STUDY 2

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GIVEN:

W/L=5u/500n=10

Y=((A+B)C)’

PERIOD

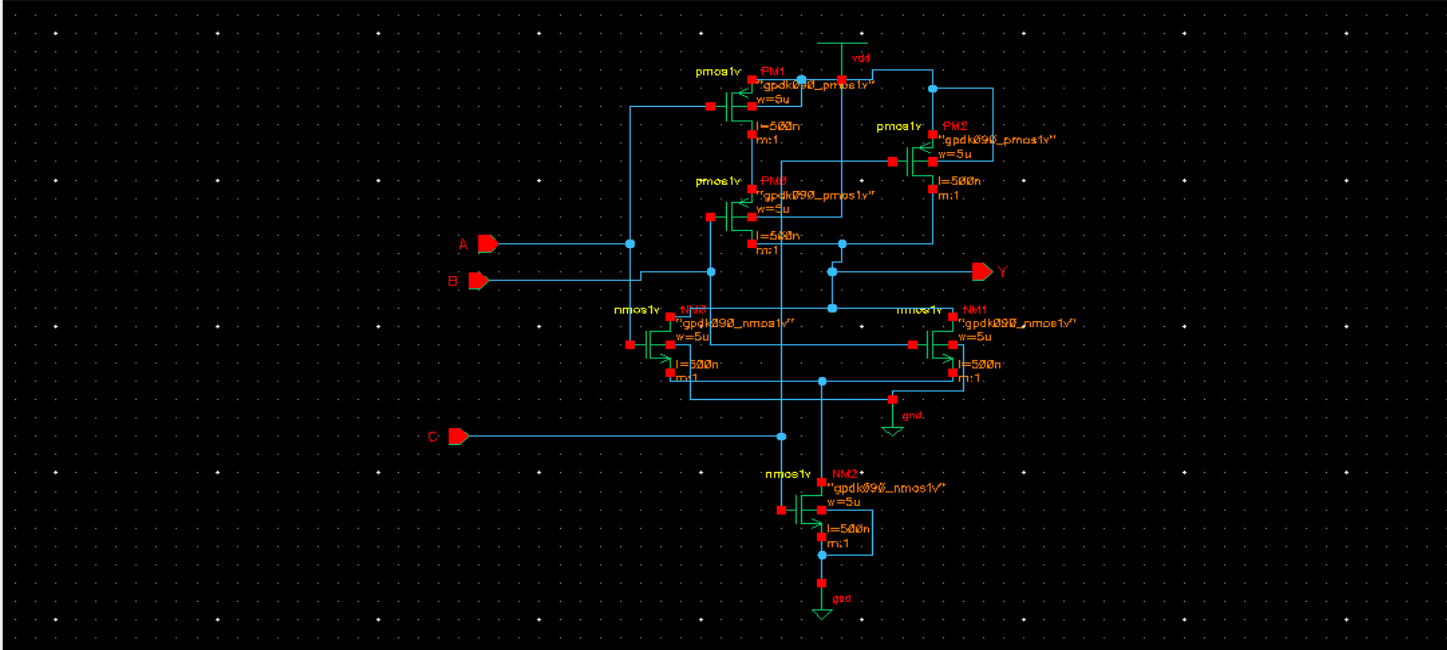
A=40ns

B=20ns

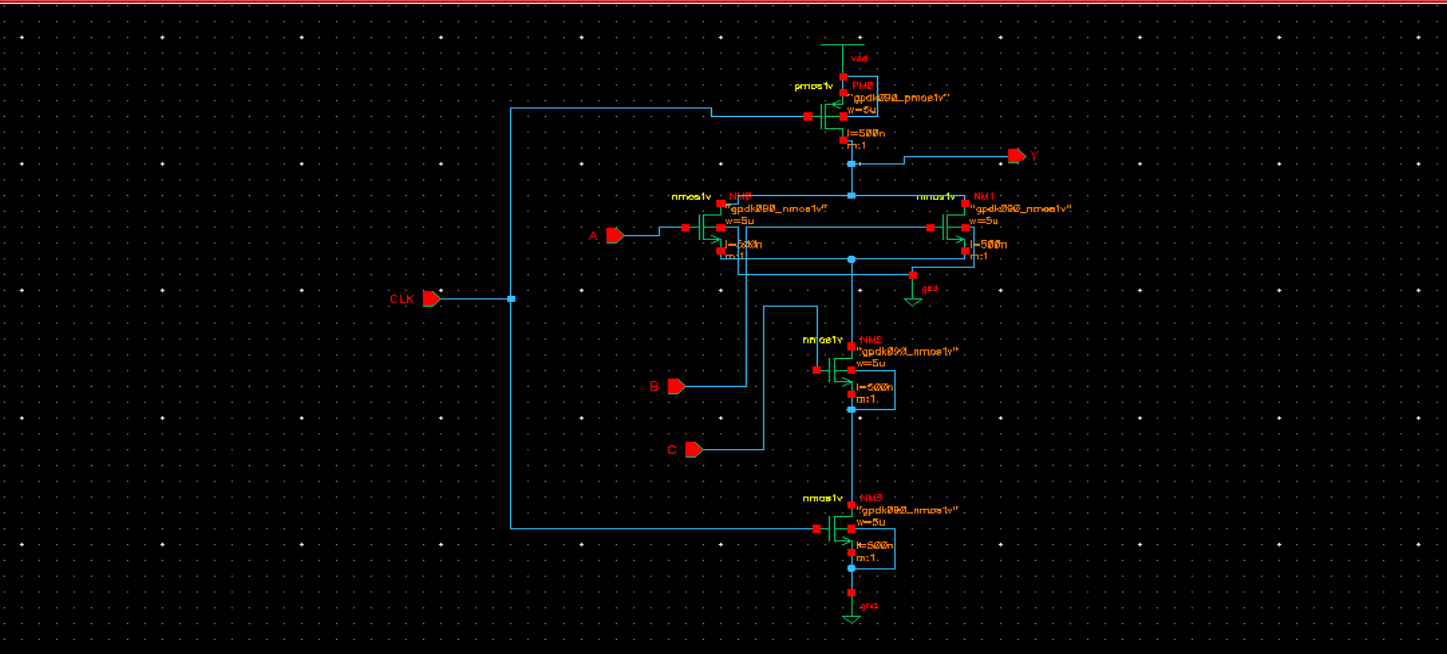
C=10ns

Clk=100MHz

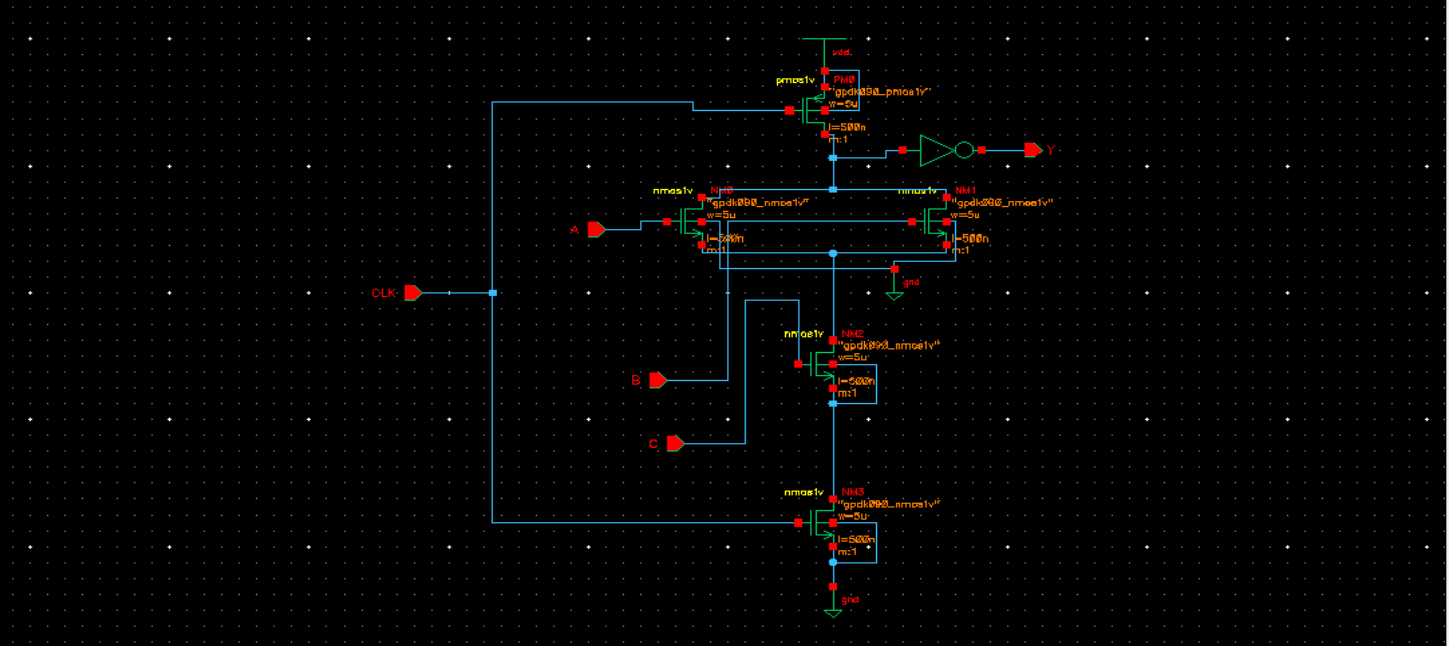
1)STATIC CMOS CIRCUIT



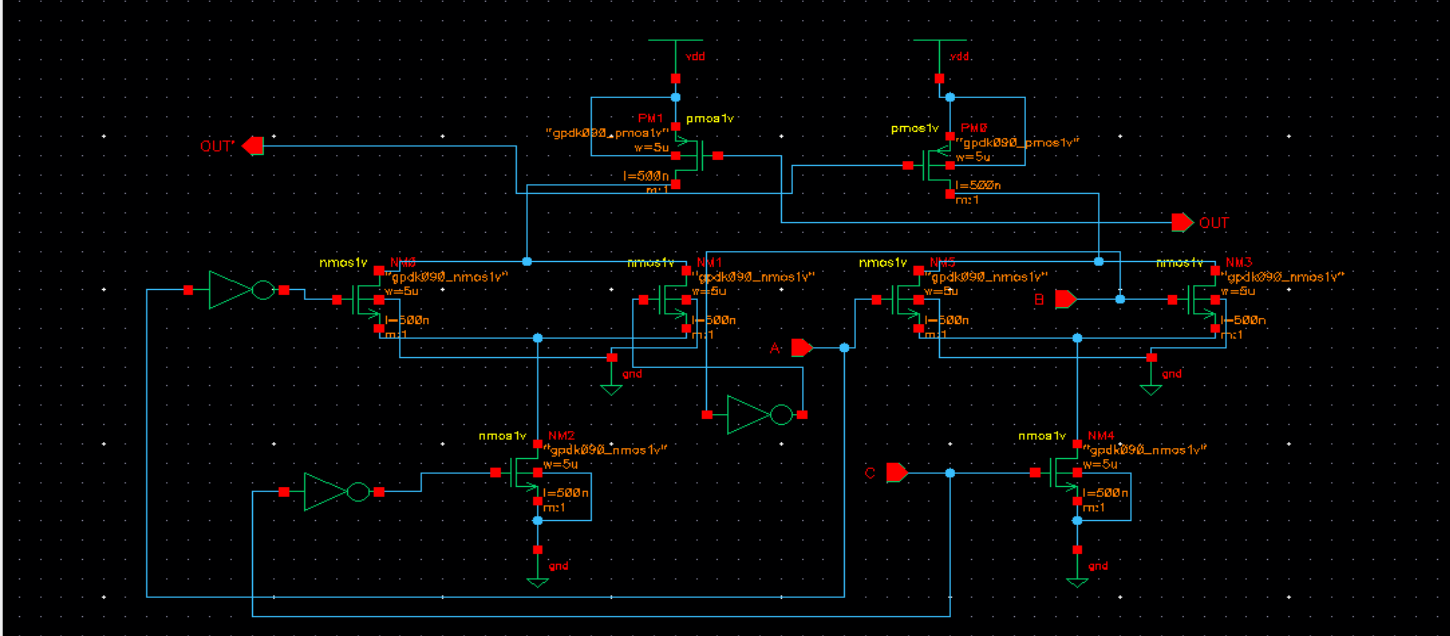
2)DYNAMIC CMOS CIRCUIT



3)DOMINO LOGIC CIRCUIT



4)CPL LOGIC CIRCUIT



POWER & DELAY ANALYSIS

|  |  |  |
| --- | --- | --- |
| CIRCUIT | POWER | DELAY |
| STATIC CMOS CIRCUIT | 104.66 u | 18ps |
| DYNAMIC CMOS CIRCUIT | 142.845u | 16ps |
| DOMINO LOGIC CIRCUIT | 178.304 u | 120ps |
| CPL LOGIC CIRCUIT | ERROR(Finding Soon) | ERROR(Finding Soon) |